

### REMARKS

Applicants have amended claims 1, 9, 10, 12, 13, 24, and 26. Claims 19-23 have been withdrawn. New claims 28-35 have been added. Applicants submit that the claim amendments are supported by the specification, and no new matter has been added.

The examiner rejected claims 1, 13, 16, 24, 26, and 27 under 35 U.S.C. 102(e) as being anticipated by Clarke.

The examiner rejected claims 2-6 and 15 under 35 U.S.C. 103(a) as being unpatentable over Clarke.

#### Claim 1 and dependent claims 2-6

Applicants submit that Clarke does not disclose or suggest "a bias circuit to provide a substantially constant voltage signal to bias at least one of the plurality of capacitors," as recited in amended claim 1. Instead, Clarke discloses capacitors that are connected to ground. Thus, claim 1 is patentable over Clarke.

Claims 2-6 are patentable for reasons similar to claim 1.

#### Independent claim 13 and dependent claim 15

Applicants submit that Clarke does not disclose or suggest "a real time clock to generate a real time clock signal having a frequency suitable for deriving a system time signal, the real time clock having a digitally tunable oscillator for digitally adjusting an operating frequency of the real time clock to speed up or slow down the system time signal," as recited in claim 13. In claim 13, the real time clock signal has a frequency suitable for deriving a system time signal.

Instead, Clarke merely discloses that the frequency of the "standard clock signal" may be adjusted. Clarke neither discloses nor suggests a "real time clock" that generates "a real time clock signal having a frequency suitable for deriving a system time signal," and that the speed of the system time signal can be increased or decreased by adjusting the operating frequency of the real time clock. Thus, claim 13 is patentable over Clarke.

Claim 15 is patentable for at least the same reasons as claim 13.

#### Claim 16

Applicants submit that Clarke does not disclose or suggest “generating a system time signal using the oscillating signal,” as recited in amended claim 16. Clarke discloses generating an oscillating signal, but does not disclose or suggest “generating a system time signal using the oscillating signal.” Thus, claim 16 is patentable over Clarke.

#### Claim 24

Applicants submit that Clarke does not disclose or suggest “a control unit to control a real time clock signal having a frequency suitable for deriving a time signal representing time, the control unit generating a set of control signals ... to control the oscillating frequency of the real time clock signal to control the time signal,” as recited in amended claim 24. Thus, Clarke is patentable over Clarke.

#### Claims 7 and 8

The examiner rejected claims 7 and 8 under 35 U.S.C. 103(a) as unpatentable over Clarke in view of Kuhn. Applicants submit that the feature of claim 1 lacking in Clarke (e.g., a bias circuit to provide a substantially constant voltage signal to bias the plurality of capacitors) is also not disclosed or suggested by Kuhn. Thus, claim 1, as well as claims 7 and 8, are patentable over Clarke and Kuhn.

#### Claims 9 and 10

The examiner rejected claims 9 and 10 under 35 U.S.C. 103(a) as unpatentable over Clarke, Kuhn, and Horn. Applicants submit that the feature of claim 1 lacking in Clarke and Horn is also not disclosed or suggested by Horn. Thus, claim 1, as well as claims 9 and 10, are patentable over Clarke, Kuhn, and Horn.

Claims 11 and 12

The examiner rejected claims 11 and 12 under 35 U.S.C. 103(a) as unpatentable over Clarke in view of Leduc. Applicants submit that the feature of claim 1 lacking in Clarke is also not disclosed or suggested by Leduc, which merely shows capacitors connected to ground (FIG. 1a). Thus, claim 1, as well as claims 11 and 12, are patentable over Clarke and Leduc.

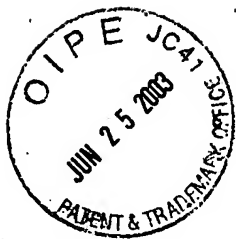
Claims 14, 17 and 18

The examiner rejected claims 14, 17, and 18 as unpatentable over Clarke in view of Theus. Applicants submit that the feature of claim 13 lacking in Clarke (e.g., a real time clock to generate a real time clock signal having a frequency suitable for deriving a system time signal) is also not disclosed or suggested by Theus, which merely shows an output signal 2a being adjusted to have the same oscillation frequency as a reference signal source 8 (col. 5, lines 3-17). Thus, claim 13, as well as claim 14, are patentable over Clarke and Theus.

The feature in claim 16 that is lacking in Clarke (e.g., generating a system time signal using the oscillating signal) is also not disclosed or suggested in Theus. Thus, claim 16, as well as claims 17 and 18, are patentable over Clarke and Theus.

Claim 25

The examiner rejected claim 25 under 35 U.S.C. 103(a) as being obvious over Horn in view of Clarke. Applicants submit that the feature of claim 24 lacking in Clarke (e.g., a control unit to control a real time clock signal having a frequency suitable for deriving a time signal representing time, the control unit generating a set of control signals ... to control the oscillating frequency of the real time clock signal to control the time signal) is also not disclosed or suggested by Horn. Thus, claim 24, as well as claim 25, are patentable over Clarke and Horn.



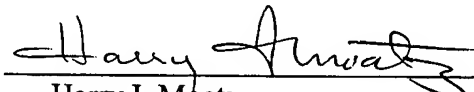
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**Expires: May 16, 2004**

  
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